

## **ACTEL ENHANCES LIBERO INTEGRATED DESIGN ENVIRONMENT FOR ITS SUCCESSFUL PROASIC<sup>PLUS</sup> FPGAS**

*Version 5.0 Offers More Than 60 Percent Performance Improvement; Adds New Ease-of-Use Features; and Extends Interfaces to Industry-Leading Tools*

**SUNNYVALE, Calif., August 4, 2003** - Actel Corporation (Nasdaq: ACTL) today introduced its new Actel Libero™ Integrated design environment (IDE) version 5.0 for the design and development of its field-programmable gate array (FPGA) families. With enhancements to the synthesis and place-and-route tools from Synplicity® and Actel, the new design suite is able to offer a more than 60 percent performance improvement for the company's successful, flash-based ProASIC<sup>PLUS</sup> family. Actel's Designer v5.0, the physical design tool suite within the Libero IDE, offers designers new features, including a comprehensive ChipPlanner for user-driven device floorplanning and a powerful Multi-View Navigator graphical interface. The Libero IDE v5.0 also features expanded interfaces to external tools, such as the Precision and LeonardoSpectrum synthesis tools from Mentor Graphics, the Synplify Pro® synthesis software from Synplicity, and Actel's programming and debugging tools.

"In today's environment, FPGA designers will not tolerate broken or confusing design flows that impact design progress. Therefore, we continue to enhance the Libero IDE with new features and capabilities to make the process as intuitive and painless as possible. Further, the new external tool interfaces allow both FPGA and ASIC users to plug their tools of choice into the flow," said Saloni Howard-Sarin, tools marketing director at Actel. "The Libero IDE v5.0 takes Actel's tool offerings to the next level with more than 60 percent performance improvements and a reduction in design cycle time when designing next-generation FPGA solutions."

### **Enhancements to the Libero Design Environment**

The Libero IDE v5.0 features Synplicity's Synplify®7.3 software, which includes several quality of results (QoR) enhancements and improved performance for Actel's FPGA families. Also included in the new version of the Libero tool suite are many functional and ease-of-use improvements via SynaptiCAD's WaveFormer Lite v9.0 and Mentor Graphics' ModelSim®v5.7 offerings.

"FPGA designers today are looking for complete integrated design environments to help accelerate their time to market," said Tom Feist, director of product marketing, FPGA Synthesis, Mentor Graphics. "By partnering with Actel, we are meeting this requirement by offering our mutual customers Mentor's industry-leading point tools,

such as ModelSim, LeonardoSpectrum and Precision Synthesis, integrated within the Libero design environment, as well as offering Actel's Designer v5.0 within our own integrated environment, FPGA Advantage."

"SynaptiCAD has continued its partnership with Actel to provide best-in-class EDA tools for designers of Actel's FPGAs," said Dan Notestein, president of SynaptiCAD. "The easy-to-use WaveFormer Lite test bench generation system fits seamlessly into the Actel Libero IDE and allows designers to meet their time-to-market goals when designing current and next-generation FPGAs."

The Actel Designer v5.0 software contains several ease-of-use enhancements, including ChipPlanner and the Multi-View Navigator. A comprehensive graphical interface for user-driven device floorplanning, ChipPlanner enables designers to achieve the best tradeoffs between optimal design density and performance through the management of regions, logic placement, I/O assignment and routing. The new Multi-View Navigator simultaneously displays ChipPlanner, Netlist, Package, I/O Attributes, Hierarchy and Log Window views, thereby offering designers a comprehensive and efficient design management methodology. Further, improvements to the Placer and Router functions in Designer v5.0 provide up to 15 percent additional performance improvements for Actel FPGAs.

### **About the Libero Integrated Design Environment**

Actel's Libero comprehensive design environment integrates industry-leading design tools and streamlines the design flow; manages all design and report files; and seamlessly passes necessary design data between tools. The Libero tool suite supports mixed-mode design entry input, giving designers the choice of mixing either high-level VHDL or Verilog HDL language blocks with schematic modules within a design.

The Actel Libero design environment includes best-in-class tools such as Mentor Graphics' ViewDraw™ schematic capture tool; SynaptiCAD's WaveFormer Lite 9.0 test bench generation system; Mentor Graphics' ModelSim 5.7 simulation and design verification software; Synplicity's Synplify 7.3 synthesis software; and Actel's Silicon Explorer verification and logic analyzer tool and Actel Designer place-and-route software.